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Single Crystalline PtSi Nanowires, PtSi/Si/PtSi Nanowire Heterostructures, and Nanodevices

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ABSTRACT

We report the formation of PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices from such heterostructures. Scanning electron microscopy studies show that silicon nanowires can be converted into PtSi nanowires through controlled reactions between lithographically defined platinum pads and silicon nanowires. High-resolution transmission electron microscopy studies show that PtSi/Si/PtSi heteorstructure has an atomically sharp interface with epitaxial relationships of Si[1$\bar{1}$0]//PtSi[010] and Si(111)//PtSi(101). Electrical measurements show that the pure PtSi nanowires have low resistivities $\sim$28.6 $\mu\Omega$·cm and high breakdown current densities >1 $\times$ 10^8 A/cm^2. Furthermore, using single crystal PtSi/Si/PtSi nanowire heterostructures with atomically sharp interfaces, we have fabricated high-performance nanoscale field-effect transistors from intrinsic silicon nanowires, in which the source and drain contacts are defined by the metallic PtSi nanowire regions, and the gate length is defined by the Si nanowire region. Electrical measurements show nearly perfect p-channel enhancement mode transistor behavior with a normalized transconductance of 0.3 mS/μm, field-effect hole mibility of 168 cm^2/V·s, and on/off ratio >10^7, demonstrating the best performing device from intrinsic silicon nanowires.

One-dimensional nanostructures, such as nanotubes and nanowires, are attractive building blocks for nanoelectronics since their morphology, size, and electronic properties make them suitable for fabricating both active nanodevice elements and device-to-device interconnects.[1–7] In particular, substantial efforts have been made for the development of nanoscale transistors based on silicon nanowires[8,9] due to their potential to replace conventional planar metal−oxide−semiconductor field-effect transistors (MOSFET) in integrated circuits[10,11] or to open new opportunities in flexible macroelectronics[12–14] and highly sensitive biosensors.[15,16] Making reliable electrical contact to individual nanowire devices is one of the key factors that determine the device performance and reliability. Lithographically defined metal contacts are most often used in silicon nanowire transistors, which is, however, limited in at least two respects: (1) the much larger size scale of lithographically defined metal contact limits the scaling potential of the silicon nanowire devices; (2) the interface states between the silicon nanowire and metal contact often lead to Fermi-level pinning and result in a relatively large Schottky barrier for the device.[17] As a result, doped nanowires with a certain doping concentration (e.g., >10^{17}/cm^3) are typically used in order to make satisfactory source drain contact, which prevent one from making high-performance transistors based on intrinsic silicon nanowires.

The formation of metal silicide nanowires and silicide/silicon heterostructures represents an interesting approach to address the above problems. Nickel silicide has been reported[18–20] and is being used as a contact material for silicon nanowire transistors.[18,21,22] Being chemically stable in ambient or oxidizing environment, platinum is an interesting interconnecting material for nanoscale electronics where surface to volume ratio is large and the surface chemical stability is important. Additionally, the formation of platinum silicide (PtSi) is of interest because it has a very low barrier height of $\sim$0.2 eV on the valence band of silicon and is an attractive choice for ohmic contacts to p-channel Si nanowire transistors.[23] Platinum silicide nanowires have been reported recently, but without detailed characterization of their properties.[24] Here, we report the formation of single crystal PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices from such heterostructures. Scanning electron microscopy (SEM) studies show that silicon nanowires can be converted into single crystal PtSi nanowires through controlled reactions between lithographically defined Pt pads

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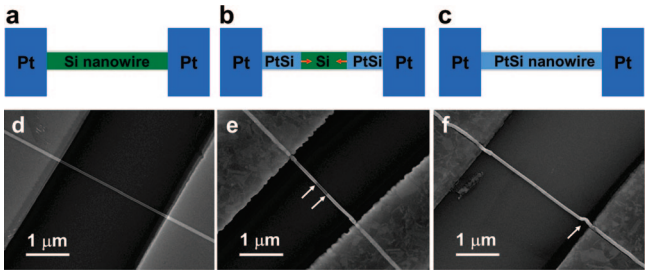

Figure 1. Formation of PtSi nanowire and PtSi/Si/PtSi nanoheterostructures. (a−c) Schematic illustrations depicting growth of a PtSi/Si/PtSi nanoheterostructure and PtSi nanowires through controlled reaction between silicon nanowires and platinum contact pads. (d) SEM image of a silicon nanowire device with two platinum contact pads before reaction. (e) SEM image of a PtSi/Si/PtSi nanoheterostructure obtained through partial silicidation of the silicon nanowire after annealing at 520 °C for 30 s. Two arrows highlight two PtSi/Si interfaces. (f) SEM image of a PtSi nanowire after complete silicidation by annealing at 520 °C for 60 s. The arrow highlights a curved section near the contact pads due to strain resulting from volume expansion.

and Si nanowires. High-resolution transmission electron microscope (HRTEM) studies show that PtSi/Si/PtSi heterostructure has clean, atomically sharp interfaces with an epitaxial relationship of Si[1$\bar{1}$0]//PtSi[010] and Si(111)//PtSi(101). Electrical measurements show that the pure PtSi nanowires have a low resistivity of ~28.6 $\mu\Omega$•cm, and high failure current density $>10^8$A/cm^2. Furthermore, using single crystal PtSi/Si/PtSi nanowire heterostructures with low PtSi/Si energy barrier, we have fabricated high-performance p-channel enhancement mode field-effect transistors from intrinsic silicon nanowires, in which the source and drain contacts are defined by the metallic PtSi nanowire regions and the gate length is defined by the Si nanowire region.

Silicon nanowires were prepared on a silicon wafer by the vapor–liquid–solid method using Au clusters as the catalyst.[25–27] The silicon nanowires are typically single crystals with diameters ranging from 30 to 60 nm, lengths greater than 10 μm, and growth axes along ⟨111⟩ directions. The Si nanowire device with platinum contacts was fabricated on Si/Si_3N_4 substrate using e-beam lithography and e-beam evaporation (Figure 1a). Prior to platinum deposition, the sample was etched in buffered hydrofluoric acid for 5 s to remove native oxide in the contact region. To allow platinum to diffuse into the silicon nanowire and form partially (Figure 1b) or fully silicidized (Figure 1c) PtSi nanowire, the device was annealed in forming gas at 520 °C with a rapid thermal processor for various periods of time. Before annealing, a SEM image of the device shows a uniform contrast along the axis of the nanowire (Figure 1d). After the device was annealed in forming gas for 30 s, clear contrast developed along the wire axis with two brighter sections emerging from both ends of the nanowire near the platinum pads (Figure 1e). A darker section remains between the two brighter sections, corresponding to the unreacted silicon nanowire. These results suggest that a PtSi/Si/PtSi nanowire heterostructure is formed through reaction between the silicon nanowire and two platinum contact pads. This is attributed to the fact that many platinum atoms are able to dissolve into silicon through the contacts between silicon nanowire and platinum pads so that supersaturation can be reached; thereby, nucleation and growth of platinum silicide occur at both platinum pads. Upon further annealing, the two brighter sections (PtSi) converged, and the darker section (Si) disappeared. At this point, all silicon is consumed and a silicon nanowire is fully transformed into a PtSi nanowire (Figure 1f). Occasionally, a curved section is seen near the contact pads (Figure 1f), which can be attributed to strain resulting from the volume expansion during the silicidation process. Transformation of Si nanowire into PtSi nanowires roughly increases the volume by 50%. However, our studies indicate that no significant diameter increase is observed (<10%). For mass conservation, this means that the silicon atom back diffusion is present in our system, in which silicon atoms diffuse toward platinum pads and get consumed in or near the pads. Additional studies are required to further understand this phenomenon.

To understand the formation and structure of the PtSi/Si/PtSi nanowire heterostructure, we have used lattice resolved transmission electron microscopy (TEM) images to determine the crystal structure and atomic epitaxial relationships. To prepare TEM samples, silicon nanowires devices were prepared on silicon grids with a square opening covered with a window of a glassy Si_3N_4 film. The thickness of the Si_3N_4 film is about 30 nm so that it is transparent to the electron beam and does not interfere with the imaging of the nanowires. Lattice resolved images were taken with a JEOL 3000F high-resolution transmission electron microscope. A high-resolution TEM (HRTEM) image (Figure 2a) shows that there are clean interfaces between PtSi/Si with an approximately 2 nm silicon oxide shell surrounding both the silicon and platinum silicide regions, suggesting the growth of platinum silicide nanowire is confined in the preformed native silicon oxide shell. On the basis of the TEM studies, the silicide material is identified to be single crystal PtSi phase with an orthorhombic structure with lattice constants $a = 0.5939$ nm, $b = 0.5596$ nm, and $c = 0.3604$ nm. A HRTEM image and its fast Fourier transform (FFT) (Figure 2b and insets) show the Si/PtSi epitaxial interface is parallel to the (111) plane of Si as well as the (101) plane of PtSi. Thus, the growth direction of PtSi is normal to the (101) plane. The crystallographic orientation relationships between Si and PtSi are Si[1$\bar{1}$0]//PtSi[010] and Si(111)//PtSi(101).

Across the epitaxial interface, the largest lattice mismatch is between the Si(002) plane ($d = 0.271$ nm) and the PtSi(200) plane ($d = 0.297$ nm) with a relative mismatch of about 8.8%. Notably, despite this exceedingly large lattice mismatch, no apparent dislocations or other defects are seen across the interface. These results demonstrate that a sharp and atomically smooth interface is obtained in our Si/PtSi nanowire heterostructure. In stark contrast, atomically uneven interfaces are often seen in previously reported PtSi thin films grown on silicon (111) surfaces due to large lattice mismatch.[28] The clean and sharp interface in nanowire heterostructures might be attributed to increased tolerance of lattice strain and the difficulty to nucleate a dislocation at nano-

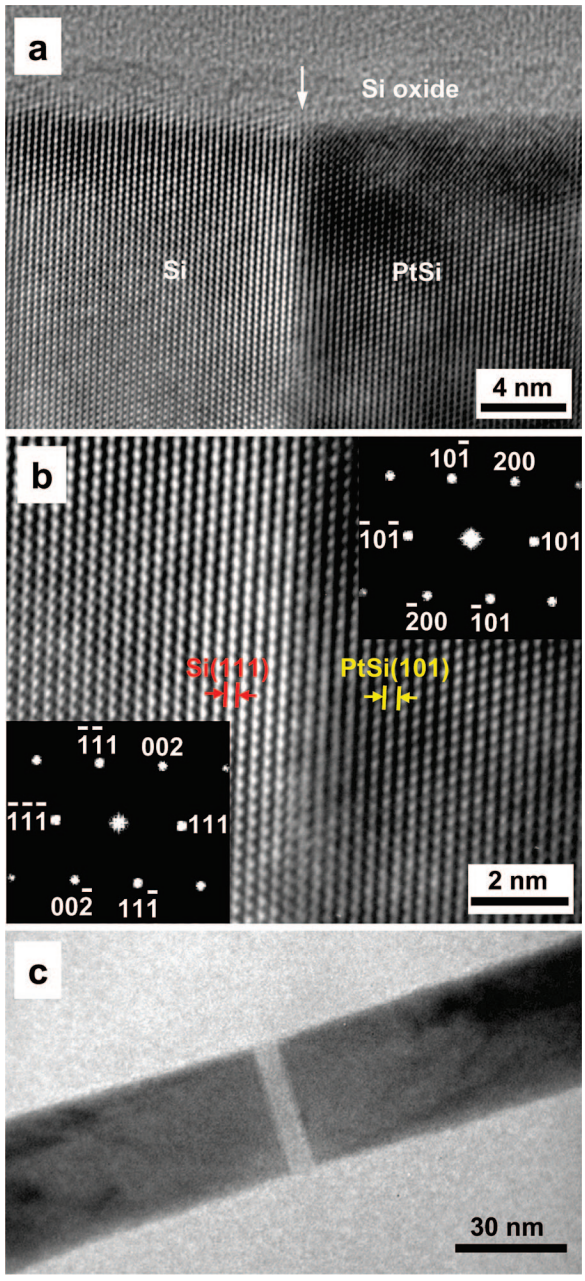

Figure 2. Epitaxial relationship of PtSi formation within a silicon nanowire. (a) A HRTEM image showing clean and sharp interfaces between PtSi and Si. The arrow highlights the Si/PtSi interface. (b) A higher magnification image of a PtSi/Si interface illustrating the epitaxial relationship. The insets are fast Fourier transform (FFT) patterns confirming the Si[1$\bar{1}$0] zone axis and PtSi[010] zone axis, respectively. (c) A TEM image of a PtSi/Si/PtSi heterostructure with only an 8 nm silicon region.

scale,[29] which is an interesting subject for further investigations.

The formation of atomically sharp PtSi/Si/PtSi heterostructures can open many exciting opportunities in nanoscale device engineering. For example, through controlled reactions, the length of the silicon region in nanowire PtSi/Si/PtSi heterostructures can be precisely controlled down to the sub-10-nm regime (Figure 2c). This is significant since the sub-10-nm length scale here is defined by controlled chemical reaction rather than by lithography and thereby can open new

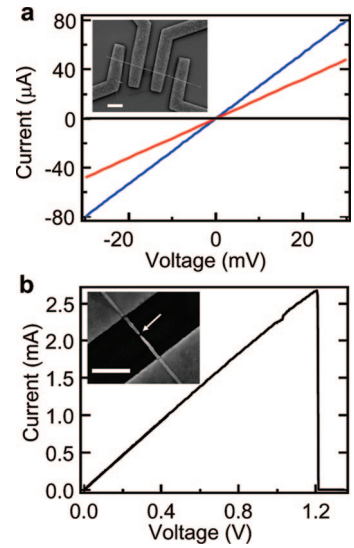

Figure 3. Electrical transport properties of single crystal PtSi nanowires. (a) Current–voltage relation recorded on a 50 nm diameter nanowire device, with the black line corresponding to the device before annealing and red line to the device after complete formation of PtSi nanowire, and the blue line to the $I-V$ relation of a four-terminal measurement which excludes the contact and lead resistance. The inset shows an SEM image of the device used for four-terminal measurement (scale bar equals 3 μm). (b) $I-V$ recorded with large applied bias voltage. The rapid drop in current at 1.2 V corresponds to the breakdown point of the PtSi nanowire device. Inset: SEM image of the nanowire after breakdown. The arrow highlights the point where breakdown occurred (scale bar equals 1 μm).

opportunities for sub-10-nm device engineering when the process is further optimized.

To explore single-crystal PtSi nanowires and atomically sharp PtSi/Si/PtSi nanoheterostructures in nanoscale electronics, it is important to understand their electrical transport characteristics. To this end, we have carried out the electrical transport studies on individual nanowires before and after PtSi formation. Current–voltage ($I-V$) measurements show that as-fabricated intrinsic Si nanowire devices with platinum contacts and partly silicidized nanowires exhibit exceedingly high resistance essentially beyond our instrument measurement range (> 1 TΩ) (black line in Figure 3a). Importantly, the fully silicidized nanowires exhibit perfect linear current–voltage relation, with current typically exceeding 100 μA at 100 mV of bias voltage. The two-terminal linear $I-V$ curve of a 50 nm PtSi nanowire device gives a linear resistance of 627 Ω (red line in Figure 3a). At this low resistance, contact resistance and electrical lead resistance may start to contribute to a significant fraction of the total resistance. To exclude this extrinsic series resistance and accurately determine the PtSi nanowire resistance, we have carried out four-terminal measurement (inset and blue line in Figure 3a), which gives a resistance of 376 Ω for the device. The high current and low resistance observed in the annealed device clearly suggest the metallic behavior of PtSi nanowires. Indeed, calculation of the PtSi resistivity based on four-terminal measurement gives a value of 28.6 $\mu\Omega$·cm. Significantly, this value compares favorably to the previously reported values in PtSi thin film materials (45–68 $\mu\Omega$·cm),[30] which can be

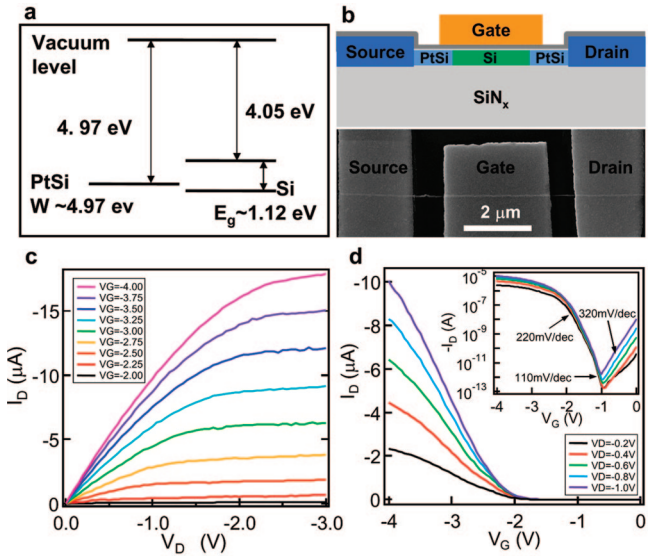

Figure 4. PtSi/i-Si/PtSi nanowire heterostructures as high-performance p-channel enhancement mode transistors. (a) Relative energy band alignment between PtSi and Si. (b) (top) Schematic of PtSi/i-Si/PtSi nanowire heterostructure device with HfO_2 as gate dielectrics. (bottom) SEM images of a device (scale bar, 2 μm). (c) Drain current (I_D) vs drain-source voltage (V_D) at increasing negative gate voltages (V_{GS}) in steps of 0.25 V starting from the bottom at $V_G = -2.0$ V. (d) I_D vs V_G at $V_D = -0.2$, –0.4, –0.6, –0.8, –1.0 V. The inset shows $-I_D$ vs V_G in the exponential scale, highlighting the on/off ratio $>10^7$, and ambipolar transport with a subthreshold swing of 110–220 mV/decade for hole transport and 320 mV/decade for electron transport.

attributed to the single crystalline and virtually defect-free structure in our PtSi nanowires as opposed to polycrystalline and defect-prone PtSi films.

To explore the PtSi nanowire as metallic interconnects for silicon nanodevices, it is also important to characterize the maximum current density of individual nanowires. Our measurement shows that an individual PtSi nanowire can typically carry more than 1 mA current before electrical breakdown. For example, the current–voltage curve of a 45 nm PtSi nanowire at large bias shows that the current reaches 2.7 mA before electrical breakdown (Figure 3b). This high current through a single nanowire corresponds to a current density 2×10^8A/cm^2, comparable to recently reported values in nickel silicide nanowires.[18] SEM observation of the failed device shows the breakdown occurs around the center of the nanowire (inset Figure 3b), where one expects the least heat dissipation and highest temperature.

The excellent electrically conductive characteristics and high breakdown current density make PtSi a natural candidate as conductive interconnects in silicon nanoelectroncs. Additionally, PtSi has a work function of 4.97 eV,[31] aligning well with the silicon valence band with a small energy barrier of ~0.2 eV and, therefore, can be used as nearly perfect ohmic contact for p-channel Si nanowire transistors (Figure 4a). Additionally, the formation of atomically clean Si/PtSi interfaces prevents Fermi level pinning and helps to maintain a low Schottky barrier determined by work function rather than by interface states.[17] This has enabled us to fabricate high-performance nanowire transistors from intrinsic silicon naowires using PtSi as the source and drain contacts. To make the device (Figure 4b), a 7 nm thick layer of HfO_2 was deposited on the surface of the partially silicidized PtSi/Si/PtSi device using atomic layer deposition process to form gate dielectrics, and a top Cr/Au electrode was defined with e-beam lithography and deposited using e-beam evaporation.

Electrical transport measurement on the device shows nearly perfect transistor characteristics. Figure 4c shows drain current (I_D) versus drain−source bias voltage (V_D) relations at various gate voltages (V_G) in steps of 0.25 V. The device shows typical p-channel enhancement mode (normally off) transistor behavior.[17] I_D increases linearly with V_D at low V_D and saturates at higher V_D. It is important to note that a nearly perfect linear relationship is observed in the I_D-V_D plot in the low bias region, which suggests that a satisfactory Ohmic contact is achieved for hole transport in the intrinsic silicon nanowire device due to a very low Schottky barrier. The plot of I_D versus V_G (Figure 4d) at constant $V_D = -0.2$, -0.4, -0.6, -0.8, and -1.0 shows little current can pass through the device when the gate voltage is below a threshold voltage of approximately -2.0 V, and I_D increases nearly linearly when the gate voltage increases in the negative direction beyond the threshold voltage.

To gauge the device performance, it is important to analyze some key device parameters including: transconductance, mobility, on/off current ratio, and subthreshold swing. High transconductance is a critical measure of transistor performance and determines voltage gains of transistor-based devices including amplifiers and logic circuits. The maximum transconductance of our device in the saturation region is ~12 μS. Assuming the effective channel width equals the nanowire diameter (40 nm), we obtain a normalized transconductance of ~0.3 mS/μm. Importantly this value is significantly better than those reported previously for chemically synthesized silicon nanowire devices and is nearly comparable to the state-of-the-art MOSFET devices (~0.6 mS/μm).[32] We note a superior value has been reported recently on nanowire transistors, which is however based on intrinsically higher mobility material (Ge/Si core−shell structure).[33] Additionally, considering the present device has a relatively long channel length (2.3 μm), the transconductance can be further improved by reducing the channel length. To estimate the carrier mobility in our nanowire device, we have modeled the device using standard MOSFET equations. In the low-bias linear region of the I_D-V_G curves, the field-effect mobility μ_h for holes can be deduced from $dI_D/dV_G = \mu_h C_G V_D/L$,[2,17] where C_G is the gate capacitance and L is the channel length. Using calculated C_G of 2.3 fF for the device, we obtain a field-effect hole-mobility of 168 cm^2/V•s, which is closely comparable to p-type single crystal silicon materials such as silicon-on-insulator MOSFET devices (~180 cm^2/V•s).[34]

The plot of the $-I_D-V_G$ curve in the logarithmic scale (inset, Figure 4d) shows that I_D decreases exponentially below the threshold voltage, and upon reaching a minimum of ~0.2 pA, it increases again upon further sweeping the gate voltage toward the positive direction. This behavior suggests ambipolar transport, with the left branch corre-

sponding to hole transport (p-type) and the right branch corresponding to electron transport (n-type). The ambipolar transport is typical of a metal-contacted Schottky barrier MOSFET and has been previously observed in silicide-contacted silicon on insulator devices and nanowire devices.[33,35,36] The plot shows that the transistor has a maximum on/off current ratio greater than 7 orders of magnitude. The exponential decrease in current defines a key transistor parameter, the subthreshold swing $S = -\mathrm{d}V_G/\mathrm{d}\log I_D$. For the hole transport branch (left), the subthrehold swing ranges from 110 mV/decade near the current minimum to 220 mV/decade near the threshold, and for the electron transport branch (right), a constant subthreshold swing of 320 mV/decade is observed. In conventional MOSFETs, subthreshold transport is dominated by thermal emission with the swing S determined by $S = (k_BT/e)\ \ln[(10)(1 + \alpha)]$, where T is temperature, k_B is Boltzmann's constant, e is elementary charge, and α depends on capacitances in the devices and is 0 when the gate capacitance is much larger than other capacitances such as interface trap state capacitance.[17] The lowest theoretical limit for S is therefore $S = (k_BT/e)\ \ln(10)$ ~60 mV/decade at room temperature. The existence of trapping states in gate dielectrics can lead to a larger than ideal substhreshold swing. Additionally, it is also often seen that a Shottky barrier MOSFET has a larger subthreshold swing due to Schottky barrier limited carrier injection. Both gate dielectric (native silicon oxide and HfO_2) interface trapping states and the Schottky barrier may contribute to the nonideal subthreshold swing observed in our devices. In hole transport branch (p-branch), the transport near the current minimum (with subthreshold swing of ~110 mV/decade) is dominated by the thermal emission, and the transport near the threshold (with swing ~220 mV/decade) is probably more also affected by the existence of a small Schottky barrier. Therefore, the subthreshold swing can be improved by reducing the interface trapping states with improved gate dielectrics and by further reducing the effective Schottky barrier with alternative contact materials (e.g., IrSi)[23] or dopants near the contact region.[35,36] The significant larger swing (~320 mV/decade) in the electron transport branch (n-branch) is due to a much larger Schottky barrier for electron transport.[35,36]

The existence of a larger Schottky barrier for electrons than for holes can also be seen from output characteristics. The linear I_D-V_D relation (in low bias region) in hole transport (Figure 4c) suggests that a satisfactory Ohmic contact is achieved due to a very small Schottky barrier. In contrast, the output characteristics of electron transport show a highly (Figure S1 in Supporting Information) nonlinear I_D-V_D relation due to a much larger Schottky barrier. Furthermore, the on-current for electron transport is at least 1 order of magnitude smaller than the that for hole transport, suggesting a Schottky barrier limited electron transport (Figure S1 in Supporting Information). These studies signify that PtSi indeed has a very small barrier for hole transport and much larger barrier for electron transport in our nanowire device, consistent with the expected Schottky barrier height of ~0.2 eV for holes and ~0.9 eV for electrons.[23] The experimental determination of the exact barrier height, however, requires additional variable temperature measurements in future studies.

These results clearly demonstrate a high-performance p-channel enhancement mode transistor has been obtained from a PtSi/Si/PtSi heterostructure using intrinsic silicon nanowires. We note the silicon nanowire transistors have been reported in a number of previous publications.[8–15,18,21,22] However, in most of these reports, chemically doped silicon nanowires are used in order to ensure a reasonable source−drain contact and decent transistor characteristics. Therefore, most of these devices are normally on devices. Transistors based on instrinsic nanowires have been reported occasionally,[8,21,22] but often with nonlinear $I-V$ characteristics and/or limited performance due to significant energy barrier at the contact. The recently reported nanowire transistors from Si/Ge core−shell nanowires did not involve chemical doping but did use Si/Ge core−shell structure for modulation doping to ensure a good source−drain contact and high device performance.[33] The fabrication of a normally off device from intrinsic materials is important for low-power consumption and can lead to better device performance (e.g., higher mobility) due to the reduced number of ionized scatter centers. Notably, our results represent the first report of high-performance normally off transistors from intrinsic silicon nanowires.

In summary, we have grown single crystal PtSi nanowires and PtSi/Si/PtSi nanowire heterostructures. TEM studies show that the heterostructures have atomically sharp interfaces free of defects. Electrical measurement of PtSi nanowires shows a low resistivity of ~28.6 $\mu\Omega$·cm and a high breakdown current density beyond 10^8 A/cm^2. Furthermore, using single-crystal PtSi/Si/PtSi nanowire heterostructures with atomically clean interfaces, we have fabricated p-channel enhancement mode transistors with the best reported performance for intrinsic silicon nanowires to date. The ability to form single-crystal PtSi nanowires and defect-free PtSi/Si/PtSi heterostructures with controlled nanoscale dimension can open new opportunities in nanoscale device engineering.

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Supporting Information Available: Figure showing the n-type (electron transport) output characteristics of a PtSi/Si/PtSi device. This material is available free of charge via the Internet at http://pubs.acs.org.

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